CLAIMS

What is claimed is:

1. A circuit to prevent contention in logic whose input derives from a scannable register, comprising:
   (a) a register having a plurality of latches having an input signal;
   (b) control logic also having the input signal which gates the input signal to the register so that the register may have only an allowed value; and
   (c) a feedback wherein some or all of an output of the register are used to control the control logic.

2. The circuit of claim 1, wherein the allowed value is such that all the latches have a value of zero.

3. The circuit of claim 1, wherein the allowed value is such that only one of the latches has a value of one.

4. The circuit of claim 1, wherein the allowed value is such that all the latches have a value of one.

5. The circuit of claim 1, wherein the allowed value is such that only one of the latches has a value of zero.

6. The circuit of claim 1, wherein the control logic comprises an logical AND function.

7. The circuit of claim 1, wherein the logic in which to prevent contention is dynamic logic.

8. A method to perform a scan test, the method comprising the steps of:

(a) determining acceptable bit values to be scanned into a register that will prevent simultaneous switching;

(b) determining if a scan function is occurring;

(c) determining if any sequence of bits to be scanned into the register of latches is not an acceptable value;

(d) gating the sequence of bits to be scanned into the register;

(e) scanning in an acceptable value into the register;

(f) providing feedback of the bit values in the register;

(g) comparing the bit values in the register to the next bit to be scanned in; and

(h) preventing the next bit from being scanned into the register if it is not an acceptable value.

9. An apparatus for scan test, comprising:

(a) means to scan in bit values for a scan test into a register;

(b) means to determine if any of the bit values in a register will result in a scan test error;

(c) means to determine the bit values in the register during a scan test;

(d) means to provide feedback of the bit values in the register to the scan in means;

(e) means to block admission of a next bit value into the register if the next bit value will result in a scan test error.

10. A method for scan testing a register, comprising the steps of:

(a) ensuring the insertion of a "hot one" bit value into the register of n latches only every nth clock cycle.

11. A method for scan testing a register, comprising the steps of:

(a) ensuring the insertion of a "cold zero" bit value into the register of n latches only every nth clock cycle.